

**REMARKS**

Reconsideration and allowance of this subject application are respectfully requested.

The Examiner has acknowledged Applicants' claim for foreign priority under 35 U.S.C. §119. Attached herewith is a certified copy of the priority document. Acknowledgement of receipt of the certified priority document is respectfully requested.

Claims 1-16 stand rejected under 35 U.S.C. §112, second paragraph for indefiniteness. The Examiner objects to the phrase "processing an input data word" in line 1 of the independent claim, alleging that it is misdescriptive. We disagree. This language in claim 1 must be read in context: "processing an input data word containing a plurality of abutting input data values." The full preamble makes clear that an input data word contains a plurality of (possibly two) data values. The terminology "input data word" is not misdescriptive because it is clearly defined in the claim. The non-limiting example in the specification is a 32-bit data word which contains 4, 8-bit data values. Withdrawal of this objection is respectfully requested.

The Examiner further objects to the terms "may extend" in line 8, "may be generated" in line 12, and "would be" in line 17 as being indefinite. As explained in the specification, a corrupting result bit is formed in some embodiments from a carry bit which may exist when a sum is performed using one of the data values. Existence of a carry bit depends on the values involved in the sum. If a carry bit is generated, then a corrupting result bit will extend into and change a value of a second result data value.

But in cases where no bit is generated, then a corrupting result will not extend into and change a value of the second result data value. Accordingly, the terminology "may extend" was employed to cover different possible scenarios. In an effort to address the Examiner's concern, this language in claim 1, as well as in claims 14 and 15, has been amended. It is clear that this amended language is only directed to the situation when a corrupting result bit is present.

Claims 11-15 have been amended largely as proposed by the Examiner. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

Claims 1-16 stand rejected under 35 U.S.C. §103 as being unpatentable over Lee et al. This rejection is respectfully traversed.

Lee describes a parallel adding and averaging circuit including plural sub-adders that operate on sub-words of two input integers. The Examiner relies on the adder 100 illustrated in Figure 3 which includes blocking circuits 110 and 112 coupled to an adding section 102. The output sum bits  $S_i$  are each connected to a corresponding multiplexer, where representative multiplexers 121-124 are shown in Fig. 3. The multiplexers are controlled by an average signal A.

Although Lee addresses the single-instruction, multiple-data problem, Lee's processing approach is completely different from that in the present invention. Lee employs additional hardware, including blocking circuits 110 and 112, to prevent the carry signal for one data value sum propagating to the next. In this way, Lee prevents a

corrupting result bit from extending into and changing a neighboring result data value.

Consequently, Lee does not need to correct a corrupting bit result using a error correcting data word. Further, when performing an averaging calculation, (as opposed to a simple addition), Lee requires multiplexers in addition to blocking circuits to control inclusion of the carrier bits in the result.

The Examiner admits that Lee fails to disclose the claimed "corrupting result bit" and "error correcting word." Nonetheless, the Examiner argues that Lee teaches "equivalent features," referencing column 5, lines 10-36:

"[t]he least significant bit of the sum is loss. The most significant bit of the average is the carry output of the single bit adder operating on the most significant bit of the partial operands" (lines 10-13).

The Examiner then contends that it would be obvious "to design the claimed invention" because Lee "discloses an adder that can be divided into a plurality of sub-adders that perform the averaging on sub-words of the input integers in parallel as claimed."

Applicant respectfully disagrees.

The Examiner's own language that it would be obvious to "design the claimed invention" clearly signals that the Examiner is relying upon hindsight in order to reconstruct the claimed invention. "Obvious to design" is not the legal standard for obviousness under §103. Rather, there must a teaching or suggestion from the prior art to modify Lee in order to "design the claimed invention" as the Examiner proposes. *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) ("even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to

modify the teachings of that reference.") The Examiner has not made that showing in this case.

The rationale the Examiner advances is that Lee discloses a plurality of sub-adders that performs averaging on sub-words in parallel. But "a plurality of sub-adders that performs averaging on sub-words in parallel" is not all that is claimed. Nor does this quoted language address the two features that the Examiner admits are missing from Lee: the "corrupting bit result" and the "error correcting data word."

There is no suggestion in Lee to provide an error correcting data word. No other reference is applied by the Examiner which teaches this missing feature. More importantly, there is no motivation to provide an error correcting word in Lee because the corrupting bit that is corrected in the claimed invention is purposefully blocked in Lee. The Federal Circuit has found that a proposed modification that renders a prior art reference in operable for its intended purpose is inappropriate for an obviousness inquiry. *In re Fritch* 972 F.2d 1260, 1265-1266 (Fed. Cir. 1992). Lee purposefully blocks carry bit propagation and requires additional circuitry to do so. The present invention does not block carrier bit propagation—nor does it require additional circuitry. Rather, the present invention calculates an error correcting word that represents any corrupting result bit(s) and combines it with an intermediate result data word to eliminate the corruption.

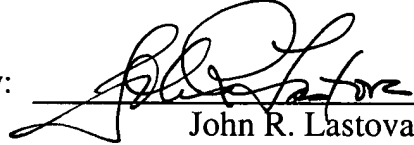
The application is now in condition for allowance. An early notice to that effect is earnestly solicited.

DIJKSTRA  
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Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By: \_\_\_\_\_

A handwritten signature in black ink, appearing to read "John R. Lastova", is written over a horizontal line.

John R. Lastova  
Reg. No. 33,149

JRL:at  
1100 North Glebe Road, 8th Floor  
Arlington, VA 22201-4714  
Telephone: (703) 816-4000  
Facsimile: (703) 816-4100